Remarks

Claims 1-22 are pending in the application. Claims 1-22 were rejected by the Examiner.

Claims 1-22 were rejected under 35 USC 103(a) as being unpatentable over Dobson et al. (US Patent No. 6,766,386) in view of Bashford (US Patent No. 6,629,179).

This amendment has amended claims 1, 8, 14, and 18 to require a processor to generate an indicator of completion to indicate the completion of the data transmission to the system processor as supported in the specification at page 6, lines 1-2.

Contrary to assertions made in the office action, Dobson does not teach 'a logic to receive a response (i.e. interrupt signal) from the expansion device (i.e.) target on the expansion bus (see col. 7, lines 50-55).' The claims, prior to any amendments made here, require that the network device *receive an interrupt signal from an expansion device on the expansion bus in the command path*. The claims do not require the device to 'receive a response,' but explicitly require reception of an interrupt signal.

The disclosure of Dobson at col. 7, lines 50-55 discloses the generation of a read request from the bridge to the expansion device. At col. 8, lines 1-10, the device receives a read response, not an interrupt, from the expansion device. If one attempts to equate the read response with an interrupt, further discussion in Dobson counters this argument. In Dobson, the bridge device issues an interrupt to the initiator device, separately and independently from the target device as disclosed in Dobson, col. 9, lines 21-29.

Therefore, Dobson does not teach the network device to *receive an interrupt signal from an expansion device*, a requirement of the claims prior to amendment.

Applicants have amended claim 1, 8, 14 and 18 to more clearly define that the expansion device transmit the interrupt *intended for the system processor*. This amendment clarifies that the network device must both receive an interrupt signal, not a read response, and that the expansion device directed the interrupt signal to the system processor.

In addition, Applicants agree with the Examiner that Dobson does not teach 'generate an indicator of completion insert the indicator into a transaction queue after a set of data.' Bashford does not teach or suggest these either.

Bashford does not teach a network device to *transmit the set of data to in a data path to the system processor, generate an indicator of completion to indicate the completion of the data transmission to the system processor, and insert the indicator into the transaction queue* as

amended claim 1 requires. Similar amendments have occurred with regard to claims 8, 14 and 18. As disclosed in Bashford, col. 6, lines 5-22, the data buffer 212 stores posted data written from devices for transmission to other devices. The secondary PCI agent then writes to an interrupt register to indicate completion of the data transfer. The interrupt generation logic then sends a message signaled interrupt (MSI) to the host computer via primary PCI bus 110. The writing to the interrupt register indicates completion of the write being posted to the data buffer 212 in the bridge. The writing to the interrupt register comes from the secondary PCI agent to the interrupt generation logic, not to the system processor, nor does the secondary PCI agent intend the interrupt writing for the system processor.

Further, the interrupt generation logic does not insert an indicator of completion in a transaction queue after the device has transmitted the data. Indeed, Bashford does not indicate how the data actually arrives at the system processor. As the data is written to a buffer in the bridge, it would seem that the system processor would then retrieve it.

Bashford teaches a network device, specifically a bridge device, including a first register arranged to store a set of interrupt bit numbers. After data transfer to the bridge device completes, each secondary device writes an interrupt bit number into the first register as disclosed in the Abstract. Bashford does not teach a secondary device sending an interrupt signal. As such, Bashford does not teach a bridge device receiving an interrupt signal from another device, such as a secondary device or an expansion device. This contrasts with claim 1, which requires the network device to receive an interrupt signal from an expansion device. In fact, Bashford admits that instead of receiving an interrupt signal, Bashford's bridge device generates message signaled interrupts (MSI) in response to the writing of the interrupt bit numbers to a register to facilitate interrupt processing. See Col. 3 lines 1-3, Col 1, lines 45-60. Since the bridge device in Bashford does not receive an interrupt signal, Bashford can not teach preventing the interrupt signal from reaching a system processor.

Therefore, Bashford does not overcome the deficiencies of Dobson, as discussed in detail above.

It is therefore submitted that claims 1, 8, 14 and 18 and their respective dependent claims 2-7, 9-13, 15-17 and 19-22 are patentably distinguishable over the prior art and allowance of these claims is requested.

Applicants have amended claim 18 to eliminate any possible statutory issues with the subject matter. No new matter has been added by this amendment. Prior art made of record but not relied upon has been reviewed and is not considered pertinent to the Applicants' disclosure. Allowance of all claims is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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